RAM Design Using Quantum-Dot Cellular Automata

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ABSTRACT

Quantum-dot cellular automata (QCA) is a novel and potentially attractive technology for implementing computing architectures at the nano-scale. By applying a set of simple layout rules, arbitrary circuits can be made using QCA cells. In this work, we describe the design and layout of a QCA random access memory (RAM), showing the layout of individual memory cells, as well as, a suggested layout for a 1x4 RAM. The RAM is based on a 2D grid of row addressable memory cells. Each of the memory cells in the RAM uses 158 QCA cells. Assuming that we can fabricate cells which are separated by 10nm, memory capacities of over 1.6 $Gbit/cm^2$ can be achieved. Simulations on the proposed memories were carried out using QCADesigner, a layout and simulation tool for QCA, by iteratively applying an intercellular Hartree-Fock approximation.

Keywords: Quantum cellular automata, random access memory, computational nanotechnology, QCA layout, digital design.

1 INTRODUCTION

QCA has gained significant popularity in recent years. This is mainly due to rising interest in creating computing devices at the nano-scale. At such scales, QCA has an inherent advantage over conventional integrated circuit technologies (such as CMOS) in that its performance increases as feature sizes are reduced, whereas CMOS exhibits decreasing performance with decreasing feature sizes. At this time, it is unclear whether or not this technology will replace such a firmly embedded technology as CMOS, but investigations into modeling and design have demonstrated that QCA has many powerful features some of which are not available in CMOS [1][7]. Although many fabrication challenges have still to be overcome [6][7], the simple design nature of QCA makes it attractive for investigation of new circuit topologies [10]. QCA topologies are not simple translations of standard circuit layouts; new ideas for translating standard logic units into QCA are needed. One of the interesting features of QCA is that there is no fixed connection strategy, and hence, it should be possible to apply optimization algorithms such as genetic algorithms to minimize the number of cells in a design.

This work is focused on the design and layout of a simple RAM architecture. We aim to maximize the memory density and focus on a layout that is minimal in its use of cells. Other design strategies have been proposed such as the SQUARES formalism [2], which is based on a set of reusable function blocks. Although this strategy simplifies the layout of circuits, it is not optimal in its use of cells and hence, produces large designs.

2 QCA RANDOM ACCESS MEMORY (RAM)

Unlike CMOS memory, QCA has no equivalent for "static memory". Memory storage is based on a circulating memory model similar to that proposed by the H-Memory architecture [3], which is a QCA implementation of a binary tree. The memory loop is divided into four consecutive clocking zones, each latching in succession. The stored memory continuously circulates in the loop until a write operation is performed at which time the memory is changed. Any read operation does not alter the memory.

Although serial structures such as the proposed H-Memory consume less clocking zones per bit, a parallel memory is more compatible with conventional architectures. Hence, this paper presents a layout of a conventional parallel memory architecture using QCA. The architecture is based on a simple 2D grid layout of memory cells. The rows of memory cells are addressed using a QCA decoder. The system diagram for the RAM is shown in Figure 1.

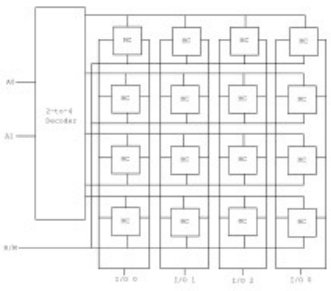

Figure 1 System diagram of QCA RAM layout.